Title: DESIGN AND VERIFICATION OF ALU BY SYSTEM VERILOG

Abstract:

This project delves into the design and verification of an Arithmetic Logic Unit (ALU) using System Verilog, a widely used hardware description and verification language. The ALU, a pivotal component in processors, executes arithmetic and logic operations, making its precise design and verification crucial. Employing System Verilog's features, the ALU is crafted with emphasis on modularity and scalability. The verification process utilizes advanced methodologies such as constrained random testing and assertion-based verification to systematically validate functionality. Integration of formal verification techniques enhances confidence in the absence of design errors. This research contributes a comprehensive methodology for designing and verifying complex digital circuits, showcasing the efficacy of System Verilog in ensuring the correctness and reliability of critical hardware components.

Outcomes:

1. A ALU is designed by system Verilog
2. All functionality is designed and verified.
3. By verifying the functionality by designing the testbench to the ALU